

1 **WHAT IS CLAIMED IS:**

2 1. A variable frequency decoding apparatus for efficient power
3 management in a portable audio device, comprising:
4 a decoder which simultaneously outputs audio information including a
5 bit rate and a sampling frequency of a data frame to a clock generator when audio
6 compressed data is received, wherein the clock generator has an input connected
7 to the decoder for receiving the audio information, such that an operation
8 frequency of the sys clock can be changed to match the sampling frequency and
9 the bit rate of the data frame for decoding with optimal performance.

10 2. The variable frequency decoding apparatus as claimed in claim 1,
11 wherein the clock generator includes:
12 a look-up table built in with a list of predetermined frequencies
13 corresponding to different bit rates and sampling frequencies used to encode
14 audio data, such that an appropriate sys clock can be simultaneously generated
15 after comparing the audio information, which is used by the decoder in decoding
16 the audio compressed data; and
17 a clock circuit which is used to generate the required sys clock with
18 predetermined frequency selected from the look-up table, to be used by the
19 decoder.

20 3. The variable frequency decoding apparatus as claimed in claim 2,
21 wherein the clock circuit in the clock generator has two outputs respectively for a
22 first and a second clock, and the two outputs of the first and second clock are
23 selectively connected to the sys clock input of the decoder and controlled by a
24 switching circuit, through which the sys clock is passed to the decoder for

1 improved efficiency.

2 4. The variable frequency decoding apparatus as claimed in claim 3, the
3 switching circuit is capable of preventing electromagnetic interference in the
4 form of glitches.

5 5. The variable frequency decoding apparatus as claimed in claim 2,
6 wherein the look-up table in the clock generator may be embedded in a
7 microprocessor.

8 6. The variable frequency decoding apparatus as claimed in claim 3,
9 wherein the look-up table in the clock generator may be embedded in a
10 microprocessor.

11 7. The variable frequency decoding apparatus as claimed in claim 4,
12 wherein the look-up table in the clock generator may be embedded in a
13 microprocessor.